Airgap Interconnects: Modeling, Optimization, and Benchmarking for Backplane, PCB, and Interposer Applications

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***Abstract*— Frequency and time domain models are developed for backplane (BP), printed circuit board (PCB), and silicon interposer (SI) links using six-port transfer matrices (*ABCD* matrices) for bumps, vias and connectors, and coupled multiconductor transmission lines for traces. The six-port transfer matrix approach enables easy computation of the transfer function, as well as near-end and far-end crosstalk. The intersymbol interference is accounted for by computing the pulse response for the worst case bit pattern. Furthermore, the models developed here are used to optimize the data-rate and trace width for each of the links, so that the aggregate bandwidth obtained per joule of energy supplied to the link is maximized. The modeling and optimization approach developed here serves as a good platform to compare the air-gap interconnects against BP, PCB, and SI interconnects on lossy dielectrics. It is shown that air-gap interconnects can provide an aggregate bandwidth improvement of 3×–4× for BP links at a comparable energy per bit, and a 5×–9× improvement in aggregate bandwidth of PCB links at the expense of 20% higher energy per bit. For SI links, air-gap interconnects are shown to provide a 2×–3× improvement in aggregate bandwidth and a 1×–1.5× improvement in energy per bit.**

***Index Terms*— Air-gap interconnects, chip-to-chip interconnects, data-rate and trace-width co-optimization, fine-pitch interconnects, silicon interposer (SI), time-domain modeling.**

I. Introduction

RECENT advances in gigascale integration have provided unprecedented computation power at the chip-level that must be complemented with high-bandwidth, low-power off-chip interconnects. Microprocessor input/output (I/O) bandwidth demands approximately double every two years [1], [2]. Hence, conventional chip-to-chip interconnects, which suffer from significant conductor and dielectric losses at higher frequencies, have become major bottlenecks in high performance nanoelectronic systems [3], [4]. Without considerable improvement in the performance and power of chip-to-chip interconnects, the boost in performance at the chip level cannot be translated to system-level improvements. Hence, many alternative technologies, including optical interconnects [5]–[7], 3-D-ICs [8]–[10], silicon interposers (SIs) [11]–[14], and air-gap interconnects [15]–[23], are being investigated. Optical interconnects have very little loss over long lengths, but due to the overhead of conversion to/from the electrical domain, they are mainly useful for longer interconnects at the backplane (BP) level in high performance servers and supercomputers [24]. Three dimensional (3-D) integration, on the other hand, aims to minimize the physical distance between the communicating ICs by stacking them on top of each other using through silicon vias. However, due to the challenges involved with heat removal from high performance 3-D-ICs, it is essential for researchers to push the performance and energy of planar interconnects to their limit. Among the novel planar interconnect technologies, SIs achieve significantly high aggregate bandwidth due to the use of very fine-pitch interconnects, whereas the performance and energy improvement in air-gap interconnects is mainly due to reduced dielectric losses and reduced capacitance. Hence, it is interesting to compare the two technologies against each other, and against the conventional links on FR-4 printed circuit boards (PCBs).

There have been numerous studies on air-gap interconnects, but they were mainly focused on process integration and reliability issues [15]–[23]. The fabrication of air-gap interconnects is done using polypropylene carbonate (PPC) as a sacrificial polymer, which thermally decomposes at higher temperatures to form the air gaps [25], [26]. Models for the reduction in capacitance or loss tangent of air-gap interconnects are available [15], [23]. However, the computation of capacitance and loss tangent are not sufficient to estimate the improvement achieved in a real system, including IO circuits. Additionally, multiple process and design constraints on both conventional and air-gap interconnects are essential for a fair comparison between the two technologies. For example,

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conventional PCB interconnects are limited by a minimum width and spacing of 4 mils (101.6 μm) [27], whereas air-gap interconnects are limited to smaller widths due to their small air-gap height for mechanical reliability. These interesting tradeoffs can be captured through a comprehensive frequency and time domain modeling approach developed in this paper. The models developed here consider multiple channel components such as bumps, vias, package traces and connectors, and noise due to intersymbol interference (ISI) and crosstalk. For fast design space exploration compared with extraction and HSPICE simulations [28], the modeling approach uses analytical models for computing the transmission line parameters. Available papers on link optimization focus either on data-rate and energy per bit [29], [30], or the estimation of maximum aggregate bandwidth as a function of data-rate and number of PCB layers [31]. However, this paper focuses on the co-optimization of data-rate and trace width to maximize the aggregate bandwidth per joule of energy supplied to the link. Although the optimization methodology was developed in [32], the modeling approach has been modified significantly to include the discontinuities like vias and bumps, realistic air-gap structures, near-end crosstalk (NEXT) and far-end crosstalk (FEXT), and timing jitter. In addition, the modeling and optimization techniques are applied to SIs and the improvement offered by air-gap interconnects for BP, PCB, and SI links are discussed.

This paper is organized as follows. Section II describes the modeling approach used in this paper, including the link architectures, parasitic extraction, and modeling for different components of the link, and frequency domain and time domain modeling techniques. The optimization methodology to simultaneously maximize aggregate bandwidth and minimize energy per bit is developed in Section III. A comparison of the aggregate bandwidth and energy of air-gap interconnects against conventional interconnects on a BP, PCB, and SI is presented in Section IV. The processes and challenges associated with the fabrication of air-gap structures are discussed in Section V. Important conclusions from this paper are summarized in Section VI.

II. Modeling Approach

The approach to modeling BP, PCB, and SI links is presented in this section. The different components of each link are described followed by an explanation of the extraction and compact models used for estimating their parasitics. The extracted parasitics and compact models are then converted to a transmission matrix form [33], such that the effective transmission matrix can be obtained by an ordered multiplication of the transfer matrices of the individual components. The effective transfer matrix is then combined with the boundary conditions to extract useful frequency domain information about the channel, including the frequency response, NEXT, and FEXT. Finally, the frequency domain information is used to obtain the time domain pulse response, NEXT and FEXT in the system. Based on certain noise assumptions and bit error rate (BER) requirements, the minimum current/voltage swing at the transmitter for reliable detection at the receiver is determined.

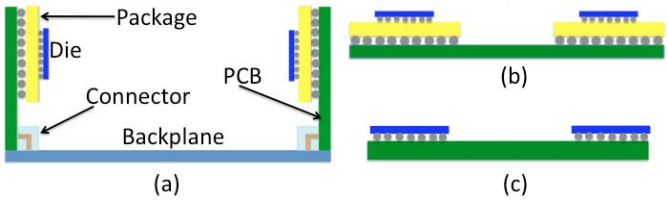

Fig. 1. Schematic view of (a) BP link, (b) PCB link, and (c) SI link.

Furthermore, the minimum current/voltage swing requirement is used to compute the power and energy per bit consumed in the transmitter. It is assumed that the current/voltage swing at the transmitter can be programmed, as demonstrated in [1].

A. Link Architectures and Interconnect Structures

In order to estimate the performance and energy gains obtained using air-gap interconnects, three different links shown in Fig. 1 are analyzed. BP and PCB links are chosen to study the impact of air-gap interconnects on long and short links, respectively. SI is a relatively new technology using very fine-pitch interconnects with high conductor losses. Hence, it is interesting to investigate if air-gap interconnects are helpful for SI links. Based on the typical link architectures for BPs and PCBs presented in [1], the links are assumed to be driven by differential current mode driver circuits and terminated at the receiver by a matched impedance. Similarly, based on the interposer link architecture presented in [14], the link is assumed to be driven by differential voltage mode circuits with high impedance termination at the receiver.

1) *BP Link:* The BP link consists of microbumps, package vias and traces, C4 bumps, PCB vias and traces, BP connectors, and BP traces. The package and PCB trace lengths are assumed to be 5 mm and 10 cm, respectively, at both the transmitter and receiver ends. The length of the BP trace is varied from 20 to 50 cm.
2) *PCB Link:* This link consists of microbumps, package and PCB vias and traces, and C4 bumps. The package traces are assumed to be 5-mm long and the PCB trace lengths are varied from 2 to 10 cm. Since the traces are short, the reflections at the vias and solder bumps are important here.
3) *SI Link:* In this case, the link consists of microbumps at the transmitter and receiver dies, and fine-pitch interconnects on a silicon carrier. The trace lengths are varied from 2 to 6 cm. Since the traces are a few micrometer wide, it is argued in [34] that the reflections from the impedance mismatch at the receiver suffer a significant round trip attenuation, thus adding negligible noise to the receiver. As a result of this mismatched impedance, the differential impedance of the traces need not be constrained to 100 Ω.

B. Extraction or Modeling of Interconnect Circuit Parameters

The approach used for the extraction and modeling of interconnect circuit parameters is described here. Initially, the link is divided into multiple physical components,

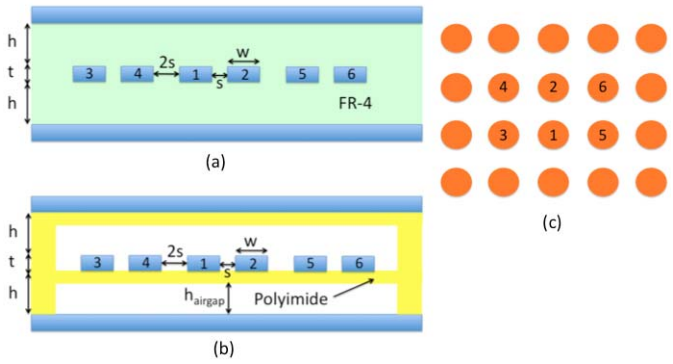

Fig. 2. Cross section of differential striplines used as the interconnect for high-speed links with (a) lossy dielectric and (b) air-gap dielectric. (c) Cross section of the package/PCB via array used for the extraction of parasitics.

e.g., the BP link could be divided into microbumps, C4 bumps, package and PCB vias, package and PCB traces, connectors, and BP traces. The two key variables used in design space exploration are data-rate and trace width. As a result, the only parasitics that depend on the design variables are those of the transmission lines used in the BP, PCB, or interposer links. The parasitics of the rest of the components do not vary with the design variables and are therefore modeled using Synopsys Raphael [35]. For this analysis, three differential pairs are considered, thus resulting in 6×6 parasitic matrices for each of the elements. Arrays of microbumps and C4 bumps are modeled using lumped capacitance matrices using 3-D Raphael. For the microbumps, the diameter and pitch are assumed to be 25 and 50 μm, respectively. For the C4 bumps, the diameter and pitch are assumed to be 250 and 400 μm, respectively. The package and PCB via capacitances are extracted using 3-D Raphael; however, since the 3-D inductance extraction is not trivial, and since the focus of this analysis is on transmission lines, the via inductance is estimated using 2-D Raphael. The inductance values obtained using 2-D Raphael are of the same order as the ones derived using simple analytical equations [36]. The package vias are assumed to have a radius of 15 μm, via–via pitch of 60 μm, and height of 50 μm, in accordance with the stack-up given in [37]. The PCB vias are assumed to have a radius of 300 μm, and a pitch of 1 mm. The connector traces are treated as transmission lines of length 1 cm, radius 300 μm, and pitch 2 mm.

The BP, PCB, and SI traces are modeled as coupled differential transmission lines, with a cross section shown in Fig. 2(a) for conventional interconnects, cross section shown in Fig. 2(b) for air-gap interconnects, and cross section shown in Fig. 2(c) for package and PCB vias. The cross-sectional dimensions chosen for the simulation of conventional and air-gap interconnects are given in Table I. Since the trace width is a key design variable, it is essential to have the capability to quickly compute the effect of varying the width on the transmission line circuit parameters. As a result, it is not a good idea to run Raphael for RLGC extraction at every design point. Instead, previously derived analytical equations from [38] and [39] are used for estimating the capacitance and frequency dependent resistance, respectively.

TABLE I
CROSS-SECTIONAL DIMENSIONS USED FOR THE SIMULATION OF CONVENTIONAL AND AIR-GAP INTERCONNECTS IN MICROMETER (w IS THE WIDTH)

	BP/PCB + FR-4	BP/PCB + Airgap	SI + SiO_2	SI + Airgap
h	304.8	23.6	3	6.6
h_{airgap}	-	20	-	3
t	17.8	17.8	3	3
s	Designed for $Z_{diff} = 100\Omega$	Designed for $Z_{diff} = 100\Omega$	0.66w	0.66w

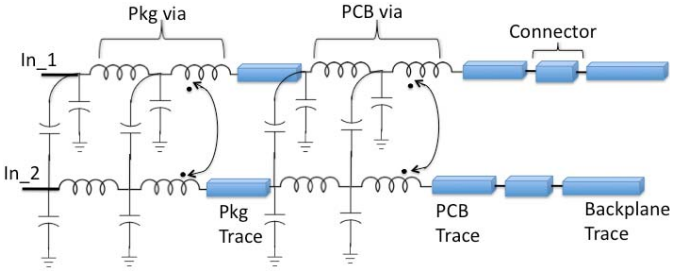

Fig. 3. Circuit model of the transmitter half of a BP channel, showing one differential pair going through pads, solder balls, package vias, package traces, PCB vias, PCB traces, connectors, and BP traces. The receiver half of the BP channel is assumed to be a mirror image of the transmitter half. The analysis includes three differential pairs, which are coupled, thus forming a six-port network for analysis.

For PCB and BP interconnects, an rms surface roughness of 0.81 μm is assumed, in accordance with [40]. The inductance matrix $[L]$ is computed from the capacitance matrix $[C]$ as $[L] = (\epsilon_r / v_0^2)[C]^{-1}$, where ϵ_r is the dielectric constant of the medium, and v_0 is the speed of light in vacuum.

C. Frequency Domain Modeling and Validation

The extracted parasitic matrices, and the analytically derived parameters for the different components are combined to form a circuit model for the six-port network representing each of the above links. The transmitter half of the circuit model of a BP channel is shown in Fig. 3. The figure just shows two out of the six lines that form the six-port network. The extracted matrices from the different components are then converted to 12×12 transfer matrices (similar to *ABCD* matrices, but with 6×6 matrices for each of the elements A, B, C, and D). The transfer matrices for the transmission lines are derived from the Resistance Inductance Conductance Capitance (RLGC) matrices using multiconductor transmission line (MTL) analysis, as shown in [33, Ch. 4]. To ensure causality in the time domain, conductor loss models given in [41] and frequency-dependent dielectric models given in [42] are used. Once the transfer matrices of each of the components are obtained, the effective transfer matrix is computed as the product of the transfer matrices of all the components. Mathematically, the voltage and current relation between the inputs and outputs is given by

$$\begin{bmatrix} [V_{\text{in}}]_{6\times1} \\ [I_{\text{in}}]_{6\times1} \end{bmatrix} = \begin{bmatrix} [\Phi_{11}]_{6\times6} & [\Phi_{12}]_{6\times6} \\ [\Phi_{21}]_{6\times6} & [\Phi_{22}]_{6\times6} \end{bmatrix} \begin{bmatrix} [V_{\text{out}}]_{6\times1} \\ [I_{\text{out}}]_{6\times1} \end{bmatrix}. \quad (1)$$

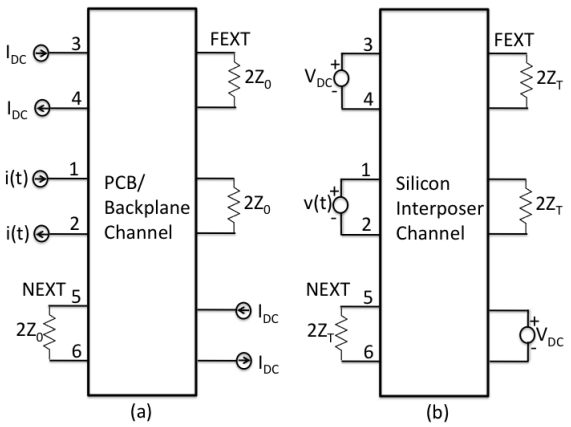

Fig. 4. Boundary conditions for (a) PCB/BP link and (b) SI link.

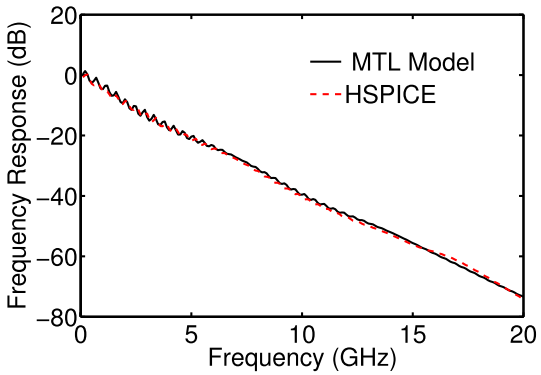

Fig. 5. Frequency response of the BP channel computed using multi-MTL models and using HSPICE.

The boundary conditions applied to the different links are shown in Fig. 4. While the BP and PCB links are assumed to be driven by differential current mode circuits and terminated with a matched impedance (100-Ω differential impedance), the SI links are assumed to be driven by differential voltage mode circuits and terminated with a high impedance (2-kΩ differential) at the receiver. By applying these boundary conditions to (1), the differential output voltage at the receiver, NEXT, and FEXT are obtained. The differential output at the receiver is given by (2) for current mode drivers, and by (3) for voltage mode drivers

$$\frac{V_{\text{out_diff_12}}}{I_{\text{in1,2}}} = Z(1,1) + Z(2,2) - Z(1,2) - Z(2,1) \quad (2)$$

$$\frac{V_{\text{out_diff_12}}}{V_{\text{in_diff_12}}} = \frac{T(1,1) + T(2,2) - T(1,2) - T(2,1)}{2}. \quad (3)$$

In the equations above, $V_{\text{out/in_diff_}xy} = V_{\text{out/in}}(x) - V_{\text{out/in}}(y)$, $[Z]$ is the matrix relating the input current to the output differential voltage, and $[T]$ is the voltage transfer matrix relating the input differential voltage to the output differential voltage given by (4) and (5). In the equations given below, $2Z_T$ is the differential termination impedance, which is assumed to be 100 Ω for BP/PCB links, and 2 kΩ for SI links

$$[Z] = \left(\Phi'_{21} + \frac{\Phi'_{22}}{Z_T} + \Phi''_{21}[M_B]\right)^{-1} \quad (4)$$

$$[T] = \left(\Phi'_{11} + \frac{\Phi'_{12}}{Z_T} + \Phi''_{12}[M_C]\right)^{-1} \quad (5)$$

$$[M_A] = \left[\Phi'''_{11} + \frac{\Phi'''_{12}}{Z_T} + Z_T\Phi'''_{21} + \Phi'''_{22}\right] \quad (6)$$

$$[M_B] = -\left(\Phi''''_{11} + Z_T\Phi''''_{21}\right)^{-1}[M_A] \quad (7)$$

$$[M_C] = -\left(\Phi''''_{12} + Z_T\Phi''''_{22}\right)^{-1}[M_A] \quad (8)$$

$$\Phi'_{xy} = \Phi_{xy}(1:4,1:4); \quad \Phi''_{xy} = \Phi_{xy}(1:4,5:6)$$
$$\Phi'''_{xy} = \Phi_{xy}(5:6,1:4); \quad \Phi''''_{xy} = \Phi_{xy}(5:6,5:6).$$

The differential FEXT, at the output ports 3 and 4 is given by (9) for current mode drivers, and by (10) for voltage mode drivers

$$\frac{V_{\text{out_diff_34}}}{I_{\text{in1,2}}} = Z(3,1) + Z(4,2) - Z(3,2) - Z(4,1) \quad (9)$$

$$\frac{V_{\text{out_diff_34}}}{V_{\text{in_diff_12}}} = \frac{T(3,1) + T(4,2) - T(3,2) - T(4,1)}{2}. \quad (10)$$

The differential NEXT, at the output ports 5 and 6 is given by (11) for current mode drivers, and by (12) for voltage mode drivers

$$\frac{V_{\text{out_diff_56}}}{I_{\text{in1,2}}} = F(1,1) + F(2,2) - F(1,2) - F(2,1) \quad (11)$$

$$\frac{V_{\text{out_diff_56}}}{V_{\text{in_diff_12}}} = \frac{G(1,1) + G(2,2) - G(1,2) - G(2,1)}{2} \quad (12)$$

where

$$[F] = \left[\Phi'''_{11} + \frac{\Phi'''_{12}}{Z_T} + \Phi''''_{11}[M_B]\right][Z] \quad (13)$$

$$[G] = \left[\Phi'''_{11} + \frac{\Phi'''_{12}}{Z_T} + \Phi''''_{12}[M_C]\right][T]. \quad (14)$$

To construct the HSPICE circuit model shown in Fig. 3, the parasitics of different components, such as pads, bumps, and package and PCB vias, are extracted using Synopsis Raphael. The RLGC parameters of the transmission lines are then computed for the structure shown in Fig. 2(a) and fed into the HSPICE W-element model. The frequency response of a 50-cm BP link obtained using the MTL model and HSPICE is shown in Fig. 5, whereas the NEXT and FEXT are shown in Fig. 6. The results obtained with the MTL models match the results from HSPICE simulations, with minor differences due to the differences in the frequency-dependent circuit parameters in the MTL model and the W-element model in HSPICE.

D. Time Domain Modeling and Validation

The frequency domain models developed in the previous section are used to obtain the pulse response of the system. The input to the system is assumed to be a periodic pulse train with a time period T_P, a finite rise/fall time T_R, and a

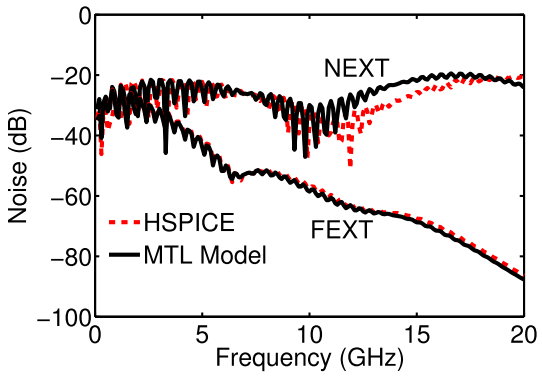

Fig. 6. NEXT and FEXT in a BP channel computed using MTL models and HSPICE.

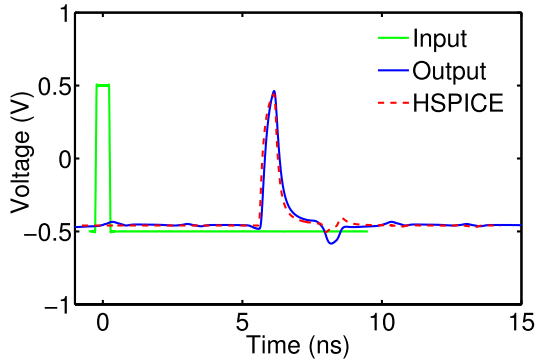

Fig. 7. Time domain pulse response of a BP link with a trace of length 50 cm, computed using six-port MTL models and HSPICE.

bit period $T_B = 1/\mathrm{DR}$, where DR is the data-rate. Thus, the Fourier series of the input pulse train is given by

$$\mathrm{in}(t) = \frac{T_B}{T_P} + \sum_{n=1}^{n=N_{\max}} a_n \cos\left(\frac{2\pi nt}{T_P}\right) \tag{15}$$

$$a_n = \frac{2T_P}{\pi^2 n^2 T_R} \sin\left(\frac{\pi nT_B}{T_P}\right) \sin\left(\frac{\pi nT_R}{T_P}\right) \tag{16}$$

where $N_{\max}$ is the maximum number of harmonics used for building the time domain pulse. To emulate the worst case scenario for ISI (a string of 0s followed by a 1), the bit period is chosen such that $T_P \geq 10T_B$. The rise/fall time of the signal is assumed to be 10% of the bit period. A four-tap finite-impulse response filter at the transmitter end is assumed to equalize the low pass channel. If $H(f)$ is the complex frequency response of the system, including the equalizer, its time domain response to the pulse (15) is given by (17). The pulse responses obtained with the model and HSPICE are shown in Fig. 7. The model developed here matches very well with HSPICE simulations

$$\mathrm{out}(t) = \frac{T_B H(0)}{T_P} + \sum_{n=1}^{n=N_{\max}} a_n \left|H\left(\frac{n}{T_P}\right)\right| \cos\left(\frac{2\pi nt}{T_P} + \angle H\left(\frac{n}{T_P}\right)\right). \tag{17}$$

Based on the estimated time of flight and a timing jitter of 30% of the bit period, the voltage at the input of the receiver is computed. Similarly, the worst case NEXT and FEXT voltages are also computed. In addition to crosstalk, some fixed noise sources at the receiver, such as receiver offset and receiver sensitivity, along with a noise margin to achieve a BER of 10^{-12} specified in [3], are considered, resulting in an effective voltage margin of 46 mV. Depending on the quality of the receiver and BER requirements, the voltage margin can change; however, any change in the voltage margin just scales the current/voltage requirement and does not significantly affect the optimization and the conclusions. For a current mode driver, the minimum current and power required at the transmitter are given by

$$I_{\min} \geq \frac{V_{\mathrm{margin}}}{\left(v_{\mathrm{out_diff_12}} - v_{\mathrm{next}} - v_{\mathrm{fext}}\right)|_{I_{1,2}=1\mathrm{Amp}}} \tag{18}$$

$$P_{\mathrm{tot}} = E_{\mathrm{pre}}\mathrm{DR} + V_{\mathrm{DD}} I_{\min} \tag{19}$$

where V_{DD} is the I/O supply voltage assumed to be 1.2 V, and E_{pre} is the energy consumed in the predriver circuits and DR is the data-rate. The main component of power consumed in the predriver circuits is assumed to be dynamic power, resulting in a constant energy per bit. To ensure a very small voltage drop across the switches, the current mode driver switches are designed for a resistance of 5 Ω and the voltage mode switches are designed for 10 Ω at the 22-nm predictive technology node [43]. This results in a predriver energy of 0.207 pJ for current mode drivers and 0.115 pJ for voltage mode drivers. For voltage mode driver circuits, the minimum voltage and power at the transmitter are given by

$$V_{\min} \geq \frac{V_{\mathrm{margin}}}{\left(v_{\mathrm{out_diff_12}} - v_{\mathrm{next}} - v_{\mathrm{fext}}\right)|_{V_{\mathrm{in_diff_12}}=1V}} \tag{20}$$

$$P_{\mathrm{tot}} = E_{\mathrm{pre}}\mathrm{DR} + \int_{t=0}^{t=4T_B} v_{\mathrm{in_diff_12}}(t) i_{\mathrm{in}_{1,2}}(t) dt. \tag{21}$$

III. Co-Optimization of Data-Rate and Trace Dimensions

A technique to optimize the data-rate based on energy per bit is presented in [29] and [30]. However, these studies assume the aggregate bandwidth of the link to be fixed and hence do not put constraints on the total routing width available. As a result, the cross-sectional dimensions of the traces are assumed to be fixed. In this paper, the goal is to co-optimize the data-rate of the link and cross-sectional dimensions of the traces. For a fixed routing width available on a PCB, a BP, or an interposer, the goal is to maximize the aggregate bandwidth, while simultaneously minimizing the energy consumed to transmit one bit over the channel. For example, if the wires are too narrow, the conductor losses in the channel are high, forcing the link to consume more energy and also operate at lower data-rates (per wire). On the other hand, if the wires are too wide, not many wires can fit in the given routing width, thus resulting in a lower aggregate bandwidth. Similarly, operating the link at high data-rates increases the aggregate bandwidth, at the expense of higher energy consumption. This section develops a systematic approach to study the above tradeoff to maximize the aggregate bandwidth per joule of energy supplied to the link.

A. Key Metrics-Bandwidth Density and Energy per Bit

1) *Bandwidth Density:* It is the aggregate bandwidth of the link per unit routing width. Mathematically, bandwidth density (BWD) can be defined as

$$\text{BWD} = \frac{\text{DR}}{p} \tag{22}$$

where DR is the data-rate and p is the pitch. This metric highlights the tradeoff between the aggregate bandwidth and available routing width.

2) *Energy per Bit:* It is the total energy required to transmit one bit of information reliably over a channel within a specified BER. Mathematically, energy per bit can be expressed as

$$\text{EPB} = \frac{P_{\text{tot}}}{\text{DR}} \tag{23}$$

where P_{tot} is the total power dissipated at the transmitter end to transmit one bit reliably, and DR is the data-rate. The total power includes the dynamic and static power dissipated in the driver, predriver buffers, and equalizers. Since the voltage margin of the signal at the receiver is fixed, the receiver power is assumed to be independent of the channel response; hence, it is not included in the analysis.

3) *Compound Metric:* BWD and EPB are two independent metrics that give an estimate of system performance and energy, respectively. However, the goal is to co-optimize system performance and energy, rather than focus on system performance or power independently. As a result, a compound metric BWD/EPB, which gives equal importance to both power and performance, is used. For a fixed routing width available on a PCB, the BP, or an interposer, this compound metric gives an estimate of the aggregate bandwidth obtained per joule of energy supplied to the link. In general, a compound metric ($\text{BWD}^{\alpha}/\text{EPB}^{2-\alpha}$) can be used to give priority to either BWD or energy per bit, based on the application.

B. Optimization Methodology

A methodology based on co-optimization of performance and energy, similar to that developed in [32], is presented here. As discussed in Section III-A, a compound metric that gives equal importance to both performance and energy (BWD/EPB) is maximized as a function of data-rate and interconnect width. The importance of using the compound metric, as opposed to either BWD or energy per bit, is also discussed in this section.

For the purpose of this optimization, the trace width and data-rate per wire are assumed to be independent variables and the circuit limit to the data-rate is assumed to be 50 Gb/s. The metrics, normalized to their maximum value in the range of data-rates, are shown in Fig. 8. For a given trace width, the BWD increases linearly with data-rate. However, energy per bit is not a monotonic function of data-rate. At low data-rates, the minimum current/voltage swing required to transmit a signal reliably over the channel depends more on the noise in the channel, and is almost independent of the loss in the channel. As a result, the total power is almost independent of data-rate; hence, the energy per bit is very high at low data-rates in accordance with (23). However, the channel losses increase with data-rate, and beyond a certain data-rate defined by the channel bandwidth, the voltage swing requirement increases rapidly with data-rate. This gives rise to an interesting bathtub-curve dependence of energy per bit on data-rate, similar to the experimental results shown in [1]. The flat region of the bathtub-curve implies that the data-rate can be increased for a small penalty in energy per bit, up to the point where the energy per bit becomes prohibitively large. Mathematically, this optimal data-rate can be chosen by maximizing the compound metric BWD/EPB, as shown in Fig. 8. Thus, by maximizing the compound metric, we can get a significant increase in data-rate for a small penalty in energy per bit.

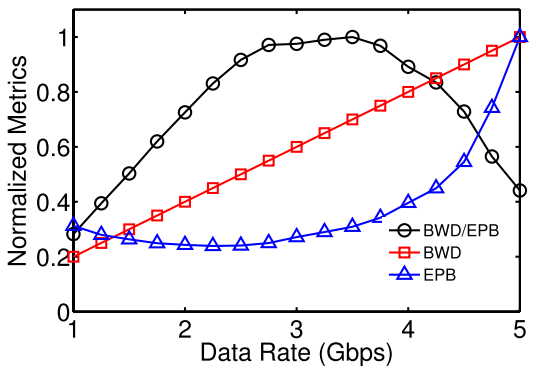

Fig. 8. Normalized metrics—BWD, energy per bit, and compound metric as a function of data-rate for a BP link with a trace width 114.3 μm (optimal width from Fig. 9) and length 100 cm.

For the BP and PCB trace-width optimizations, the spacing is varied as a function of the width to keep the differential impedance constant at 100 Ω. However, since links on a SI do not necessarily use a matched termination [14], the spacing is assumed to be two-thirds of the linewidth. The metrics, normalized to their maximum value in the range of trace widths, are shown in Fig. 9. At a fixed data-rate, increase in trace width results in an increase in pitch that leads to a reduction in BWD. However, due to the reduction in conductor loss, energy per bit decreases with an increase in trace width. Since the BWD and EPB decrease at different rates with an increase in trace width, there exists an optimal width that maximizes the compound metric, as shown in Fig. 9. Additionally, conventional PCB and BP traces are further limited by minimum width and spacing of 4 mils (101.6 μm) [27]. Thus, for conventional PCB and BP traces, optimal widths below 4 mils are rounded off to 4 mils, as shown by the shaded area in Figs. 9 and 11. However, the air-gap interconnects are not limited by this minimum width requirement [25].

The above optimization methodology gave equal importance to both aggregate bandwidth and energy per bit. However, the parameter α for the compound metric can be varied to give priority to either BWD or energy per bit. If $\alpha > 1$, a higher priority is given to BWD, thus resulting in a higher optimal data-rate and lower optimal width, as shown in Figs. 10 and 11,

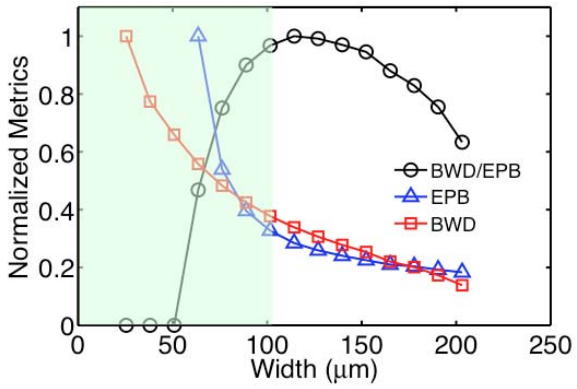

Fig. 9. Normalized metrics—BWD, energy per bit, and compound metric as a function of trace width at a data-rate of 3.5 Gb/s (optimal data-rate from Fig. 8), for a BP link with a trace length of 100 cm. Green area: widths that cannot be achieved with conventional PCB fabrication.

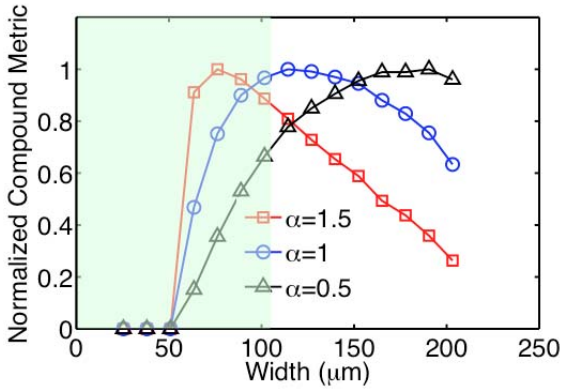

Fig. 11. Normalized compound metric $\text{BWD}^{\alpha}/\text{EPB}^{2-\alpha}$ as a function of trace width for different values of parameter α, which decides the relative importance of BWD and energy per bit for the system. The length of the BP trace is 100 cm. Green area: widths that cannot be achieved with conventional PCB fabrication.

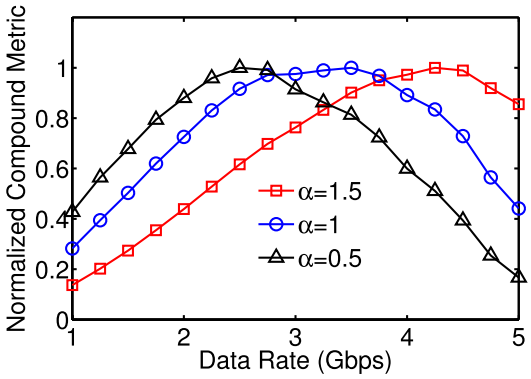

Fig. 10. Normalized compound metric $\text{BWD}^{\alpha}/\text{EPB}^{2-\alpha}$ as a function of data-rate for different values of parameter α, which decides the relative importance of BWD and energy per bit for the system. The length of the BP trace is 100 cm.

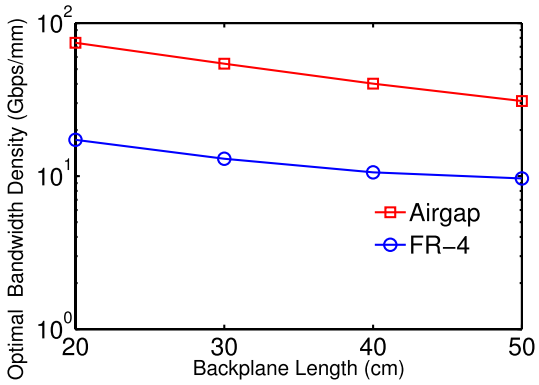

Fig. 12. Optimal BWD of a BP link with conventional FR-4 BP and air-gap BP.

respectively. Similarly, if $\alpha < 1$, a higher priority is given to energy per bit, thus resulting in a lower optimal data-rate and a higher optimal width, as shown in Figs. 10 and 11, respectively.

IV. Performance and Energy Benchmarking of Air-Gap Interconnects

In this section, the frequency and time domain models developed in Section II, and the optimization methodology developed in Section III are applied to study the impact of using air-gap interconnects for BP, PCB, and interposer applications. For each trace length, the simulations are run to compute a 2-D matrix of the compound metric BWD/EPB as a function of trace widths and data-rates; the trace width and data-rate that maximize BWD/EPB are chosen as the optimal values. As a result of using analytical models for the RLGC parameters of transmission lines in the system, the simulations are very fast compared with extraction using Raphael followed by HSPICE simulations; hence, it is possible to run the numerous simulations necessary to explore the entire 2-D design space.

A. Airgap Interconnects for BPs

The focus of this section is on the improvement obtained by using air-gap interconnects for BP links. The BP link consists of multiple components discussed in Section II-A. The PCB/BP dielectric material is FR-4, with a dielectric constant of 4.4 and a loss tangent of 0.02. The optimal BWD as a function of trace length for FR-4 and air-gap interconnects is shown in Fig. 12. The optimal BWD of airgap interconnects is roughly 3×–4× better compared with that of FR-4 interconnects. This is because the air-gap technology has larger optimal data-rate, as shown in Fig. 13, and a smaller dielectric height, which requires a smaller width for 100-Ω differential impedance. The optimal width for air-gap interconnects is ∼40 μm, whereas the optimal width for FR-4 BPs is the minimum width of 101.6 μm.

As shown in Fig. 14, the energy per bit for air-gap interconnects is comparable with that of FR-4 interconnects on BPs. This is because, the reduction in dielectric loss is nullified by the increase in conductor loss due to smaller width. Although air-gap interconnects on BPs do not offer any improvement in energy per bit, they offer an improvement in the compound metric (BWD/EPB), as shown in Fig. 15. Additionally, since the compound metric is the one being optimized, it shows

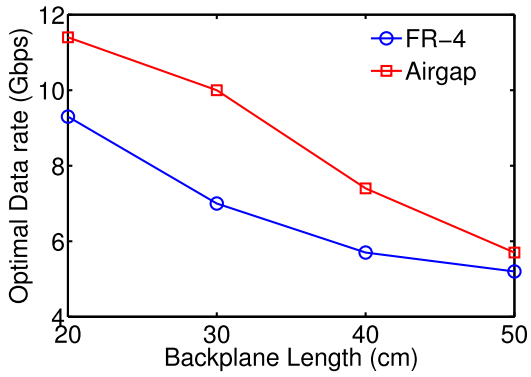

Fig. 13. Optimal data-rate of a BP link with conventional FR-4 BP and air-gap BP.

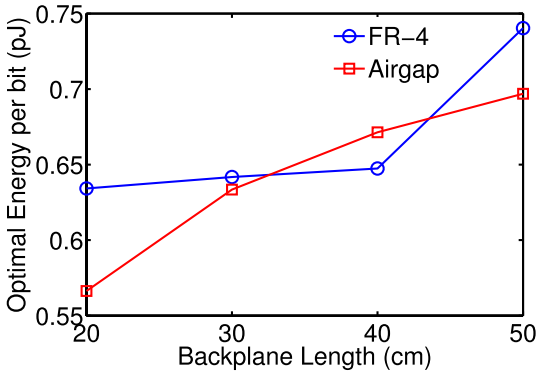

Fig. 14. Optimal energy per bit of a BP link with conventional FR-4 BP and air-gap BP.

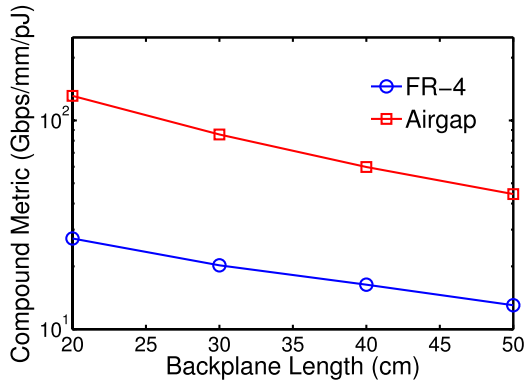

Fig. 15. Optimal compound metric (ratio of BWD and energy per bit) of a BP link with conventional FR-4 BP and air-gap BP.

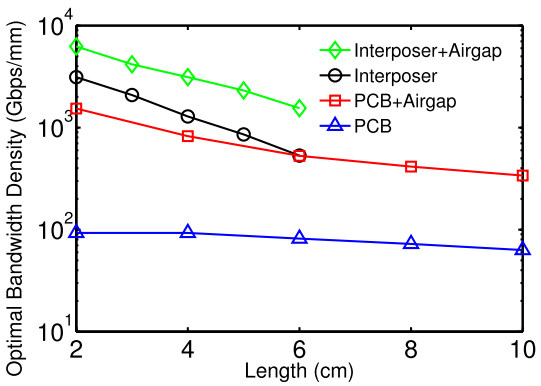

Fig. 16. Optimal BWD of a PCB/interposer link with lossy dielectrics and air-gap dielectrics.

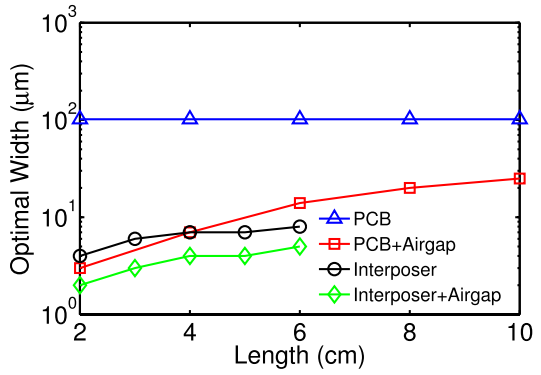

Fig. 17. Optimal trace width of a PCB/interposer link with lossy dielectrics and air-gap dielectrics.

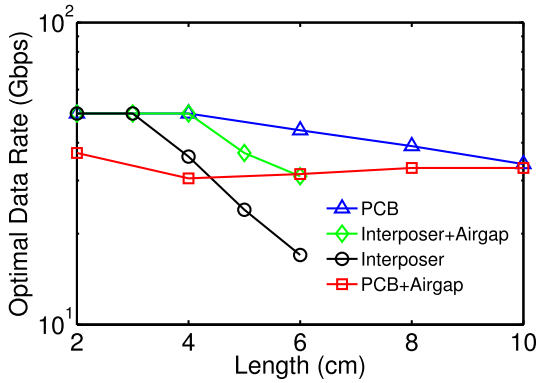

Fig. 18. Optimal data-rate of a PCB/interposer link with lossy dielectrics and air-gap dielectrics.

a monotonic decrease with an increase in the interconnect length.

B. Air-Gap Interconnects for PCBs and Interposers

The focus of this section is on the improvement obtained by using air-gap interconnects for PCB and SI links. As shown in Fig. 16, for the PCB link, the BWD of air-gap interconnects is 5×–9× better compared with that of interconnects on FR-4. Although the optimal data-rate of air-gap interconnects is smaller, as shown in Fig. 18, the much smaller optimal width (shown in Fig. 17) of the air-gap interconnects gives rise to a better BWD. However, the smaller optimal width of air-gap interconnects results in a 20% higher energy per bit, as shown in Fig. 19.

It is interesting to note that, for BP and PCB links, the improvement of air-gap interconnects degrades with an increase in the trace length. This is because, shorter wires have a higher optimal data-rate and dielectric losses are more dominant at higher data-rates. As the trace lengths increase, the optimal data-rates decrease; hence, the improvement obtained by replacing a lossy dielectric with an air-gap dielectric keeps diminishing. For SI links, the improvement of

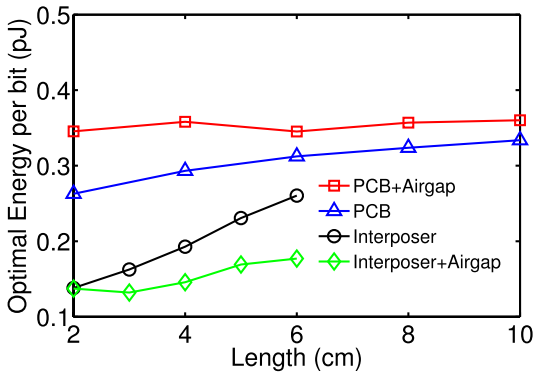

Fig. 19. Optimal energy per bit of a PCB/interposer link with lossy dielectrics and air-gap dielectrics.

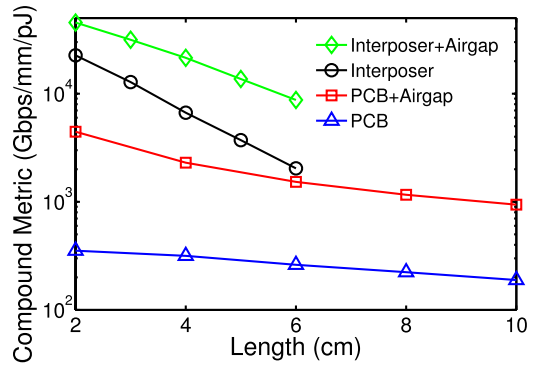

Fig. 20. Optimal compound metric (ratio of bandwidth density and energy per bit) of a PCB/interposer link with lossy dielectrics and air-gap dielectrics.

air-gap interconnects is 2×–3× in terms of bandwidth density, and 1×–1.5× in terms of energy per bit. However, since the interposer traces are not constrained to a differential impedance of 100 Ω, the improvement of air-gap interconnects in SI links is mainly due to lower capacitance. As a result, the improvement of air-gap interconnects increases with an increase in trace length. The optimal compound metrics for the PCB and SI links are shown in Fig. 20. Since the compound metric is the one being optimized, unlike other optimal metrics, it shows a monotonic decrease with interconnect length.

V. Discussion of Fabrication Processes and Challenges

The air-gap interconnect in this paper is a heterogeneous structure with differential striplines supported on a polymer membrane, where the regions between the polymer membrane and top and bottom ground planes are essentially air gaps [Fig. 2(b)]. This section gives a brief explanation about the processes involved in developing these air-gap structures and the important challenges associated with their fabrication.

A. Fabrication Process

The air-gap creation mechanism is based on the thermal decomposition of a sacrificial polymer and the diffusion of its decomposed products through a polymer membrane, thus leaving a gaseous void in place. The general processing steps of the proposed air-gap interconnect fabrication can be summarized as follows:

1) electroplating of the bottom ground plane;
2) patterning of polymer columns to create trenches for the bottom air-gap region;
3) inlay of a sacrificial polymer inside the trenches between polymer columns, i.e., bottom air-gap region;
4) coating of the polymer membrane;
5) electroplating of striplines on top of the polymer membrane;
6) patterning of another layer of polymer columns for definition of the top air-gap region;
7) inlay of sacrificial polymer inside the top air-gap region;
8) patterning of the top polymer overcoat;
9) simultaneous decomposition of the sacrificial polymer both in top and bottom air-gap regions, and curing of the polymer membrane and columns;
10) electroplating of the top ground plane.

The sacrificial polymer acts as a temporary space holder during other processing steps, and thermally decomposes to create air gaps. PPC was previously demonstrated to be a promising sacrificial polymer in air-gap transmission line fabrication on PCB substrates [44]. Air-gap structures for microelectromechanical systems packaging have been fabricated using PPC with a hybrid organic-inorganic polyhedral epoxycyclohexyl oligomeric silsesquioxanes overcoat on silicon substrates [45]. PPC thermally decomposes by photoacid catalysis in a narrow and useful temperature window completely into volatile products, which diffuse through the polymer membranes [46]. The mechanical support for striplines in Fig. 2(b) is provided by the polymer membrane, which extends to top of the polymer columns on either side of air gaps. The same solvent-cast material can be used for both the membrane and the columns, e.g., polyimide, avatrel, SU-8, and cyclotene [47].

B. Fabrication Challenges

For fabrication of air-gap structures on PCB and SI, any combination of PPC and structural polymer can be used. One important issue is the material compatibility of PPC with structural polymer, i.e., otherwise distortion of patterns by partial dissolution of polymers due to solvent transfer from one to another. In [47], it was shown that a thin layer of plasma-enhanced chemical vapor deposition-deposited SiO_2 (as small as 530 Å) on top of polycarbonate-based sacrificial polymers is successful in preventing solvent transfer between polymers without deformation of original air-gap region. However, the Coefficient of Thermal Expansion mismatch between polymers (∼30–50 ppm/K) and SiO_2 (∼0.5 ppm/K) should be considered in selecting the processing temperatures, since cracking might be observed in SiO_2 layer at high temperatures. Recently, PPC-cyclotene combination has been identified to be a fully compatible sacrificial polymer-structural polymer pair not requiring any solvent barrier layer [25]. The choice of structural polymer should be considered early in the photomask design phase, since the mechanical stability of the polymer membrane is dependent on the width of the air-gap

region, i.e., the wider the air-gap region, the more vulnerable the mechanical stability of polymer membrane, and there is a higher chance of sagging of the polymer membrane after air-gap creation [25], [45]. PPC can be thermally planarized by partial decomposition of upper layers of PPC in the air-gap region. In this case, the photomask for patterning sacrificial polymer can be widened in order to compensate for lateral photoacid diffusion into the airgap region, which can deform the air-gap pattern [25]. Any nonuniformity in the air-gap region can result in deviations in the final electrical performance of air-gap interconnect. A possible use of SiO_2 barrier layer increases the heterogeneity of the air gaps, which directly affects the dielectric loss.

VI. Conclusion

Frequency and time domain models for BP, PCB, and SI are developed here and validated using HSPICE. The models take into account ISI noise, NEXT, and FEXT, and provide a platform for the comparison of air-gap interconnects against conventional interconnects on FR-4 and SI interconnects on silicon dioxide. For BP links, the air-gap interconnects show an improvement of 3×–4× in aggregate bandwidth at a comparable energy per bit. Similarly, for PCB links, the air-gap interconnects provide a 5×–9× improvement in aggregate bandwidth at the expense of a 20% higher energy per bit. An improvement of 2×–3× in aggregate bandwidth and an improvement of 1×–1.5× in energy per bit is achieved for air-gap interconnects on a SI. For both PCB and BP links, the traces are designed for a 100-Ω differential impedance; hence, the improvement in BWD of air-gap interconnects is mainly from the reduced dielectric losses. Since the optimal data-rates are higher at smaller lengths, and the dielectric losses are more severe at higher data-rates, for PCB and BP links, the improvement in BWD of air-gap interconnects decreases with an increase in length. However, since the SI traces are not constrained to have a differential impedance of 100 Ω, their improvement mainly comes from the smaller capacitance. As a result, for the SI link, the improvement of air-gap interconnects increases with an increase in trace length.

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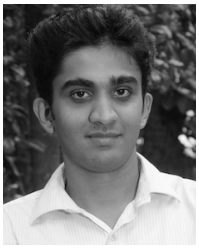

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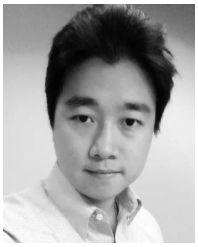

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